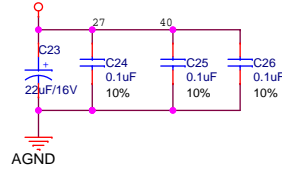


DVDD33

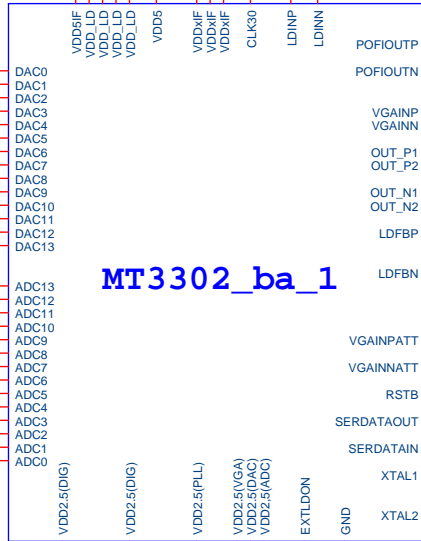


VDD-5.0VA

DVDD33

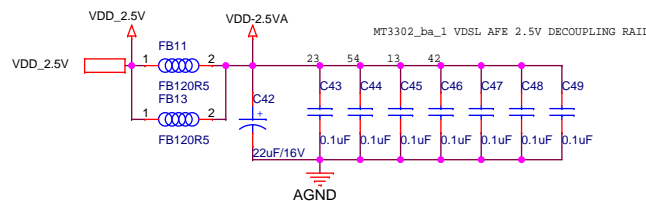
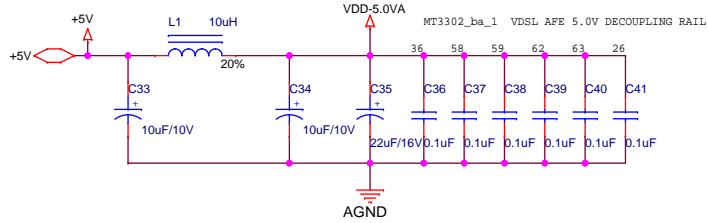
AFECUAM

R17
0R

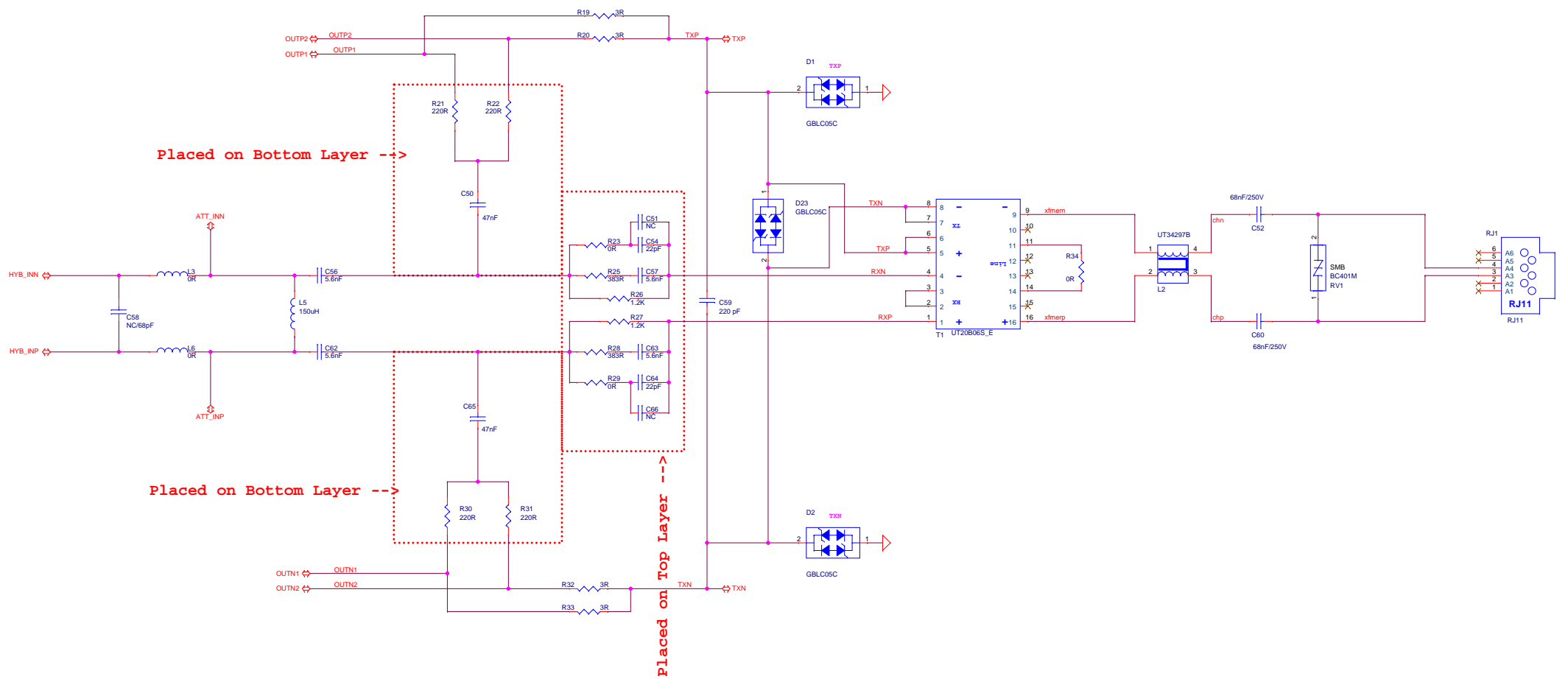


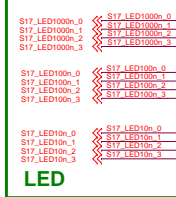
MT3302_ba_1

Internal capacitors within a range from 6pF to 38pF in about 5fF-steps at both XTAL1/2 pins. The resulting pullability to crystal are ± 200 ppm frequency range.

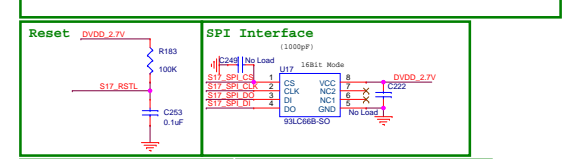
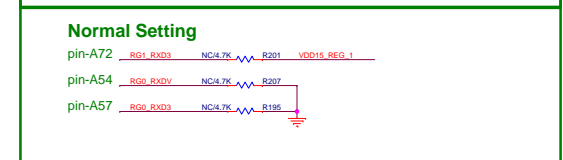
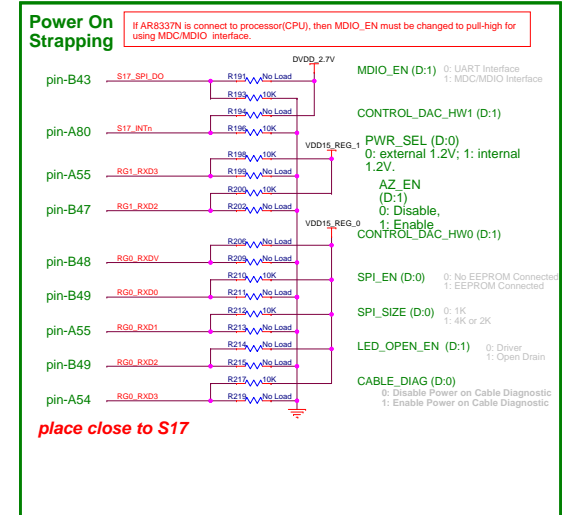
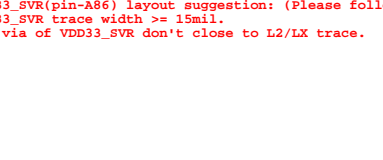
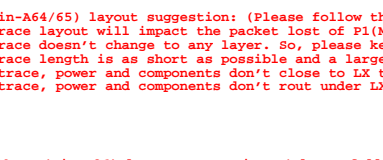
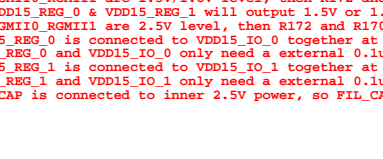
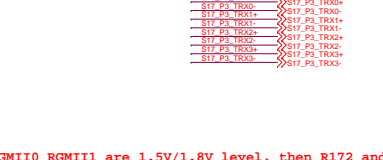
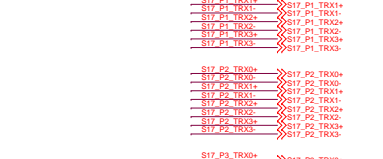
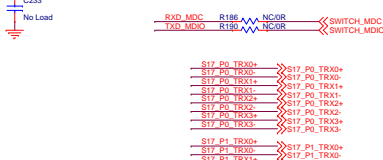
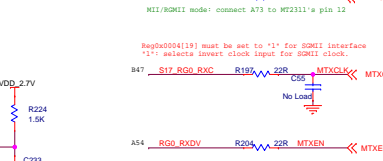
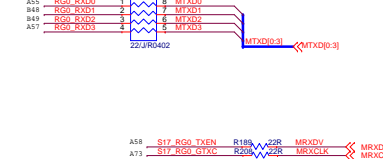
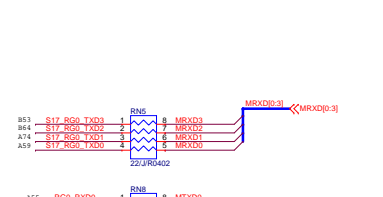
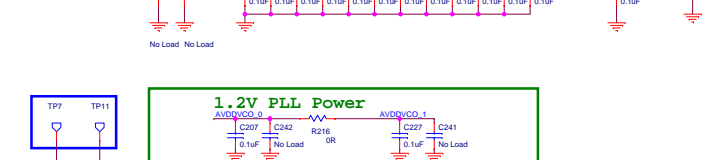
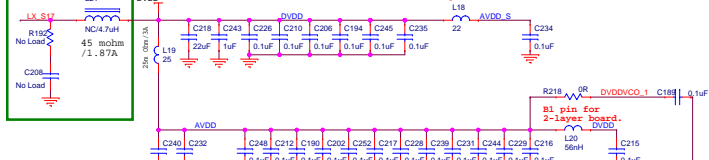
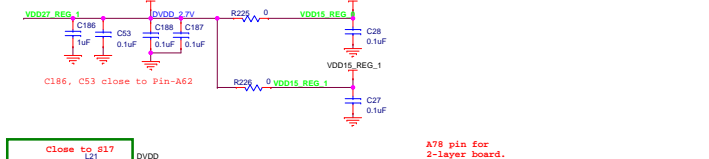
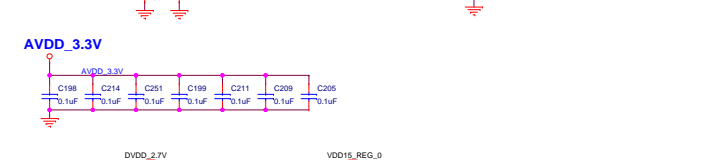
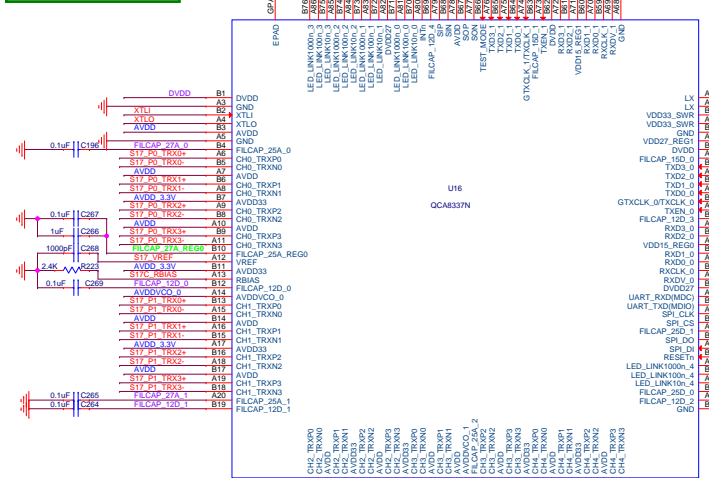


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LED



Notel:

- (1) If RGMII0, RGMII1 are 1.5V/1.8V level, then R172 and R170 are no_load.
- (2) And VDD15_REG_0 & VDD15_REG_1 will output 1.5V or 1.8V power.
- (3) If RGMII0, RGMII1 are 2.5V level, then R172 and R170 load a 0 ohm resistor.
- (4) VDD15_REG_0 is connected to VDD15_IO_0 together at S17 chip inner.
- (5) VDD15_REG_1 is connected to VDD15_IO_1 together at S17 chip inner.
- (6) VDD15_REG_0 and VDD15_IO_0 only need a external 0.1uF.
- (7) VDD15_REG_1 and VDD15_IO_1 only need a external 0.1uF.
- (8) FIL_CAP is connected to inner 2.5V power, so FIL_CAP only need a external 0.1uF.

Note 2:

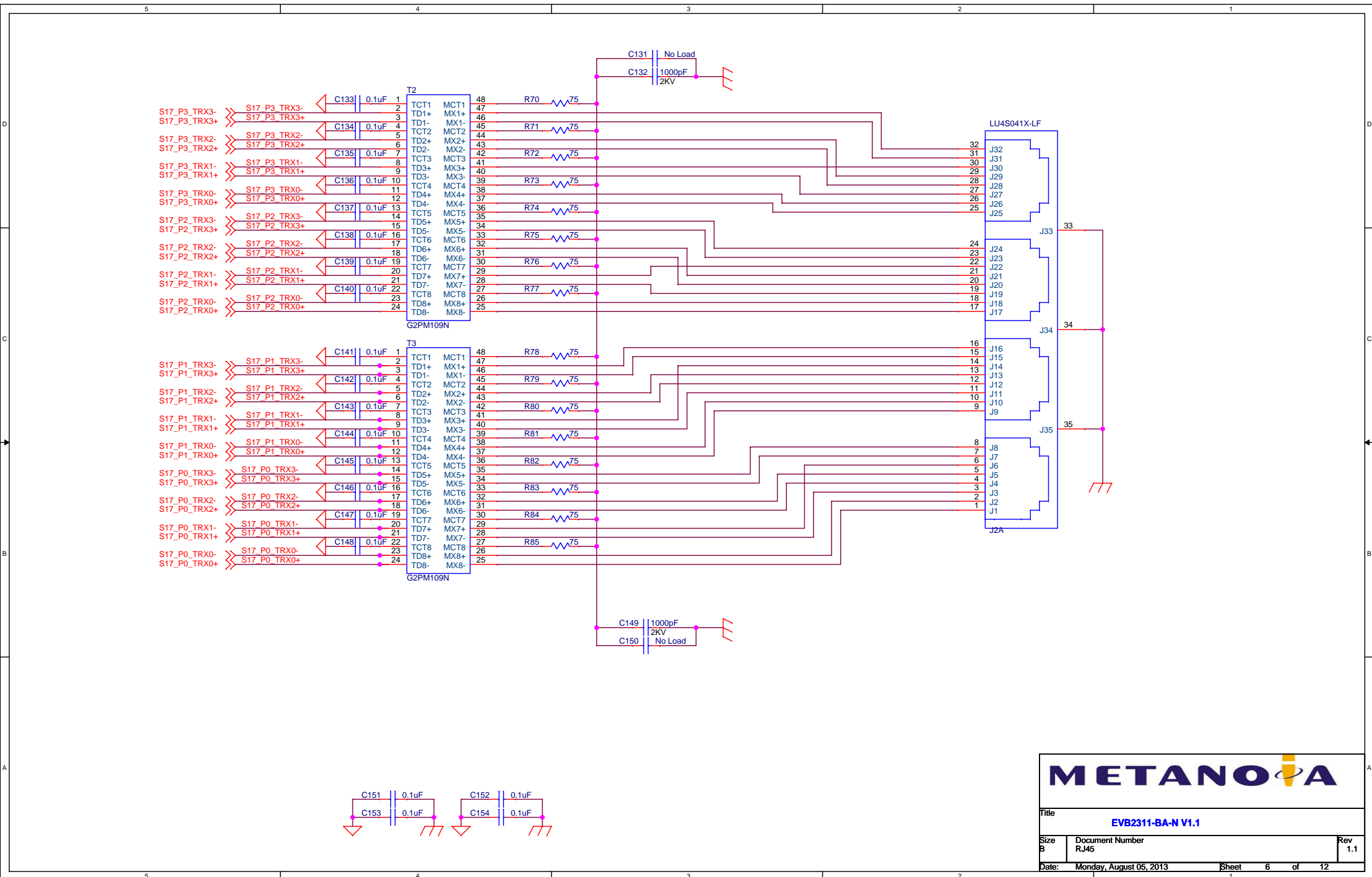
For LX(Pin-A64/65) layout suggestion: (Please follow the below suggestion)

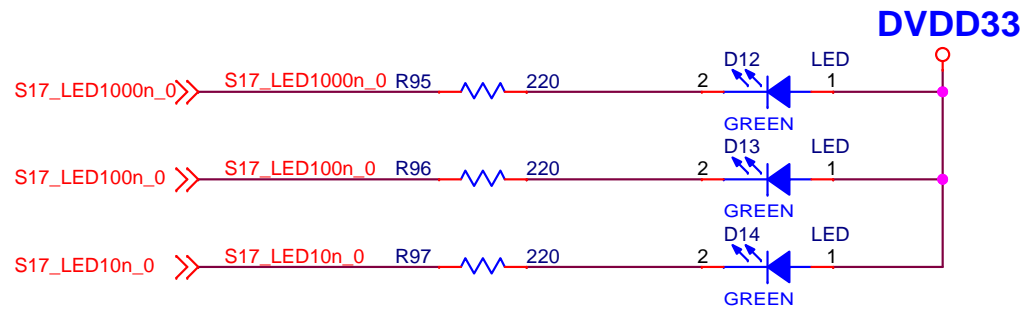
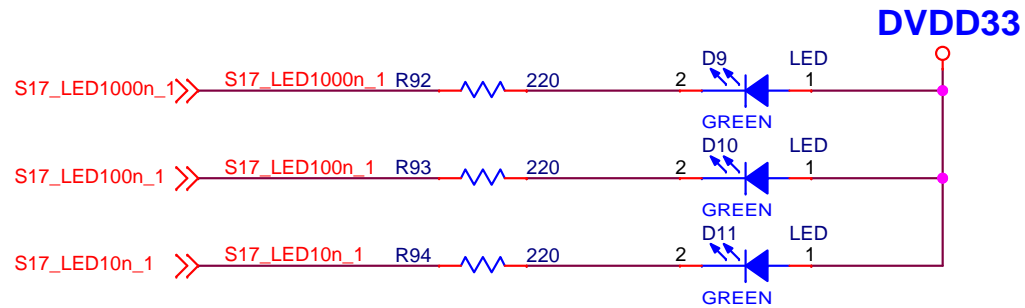
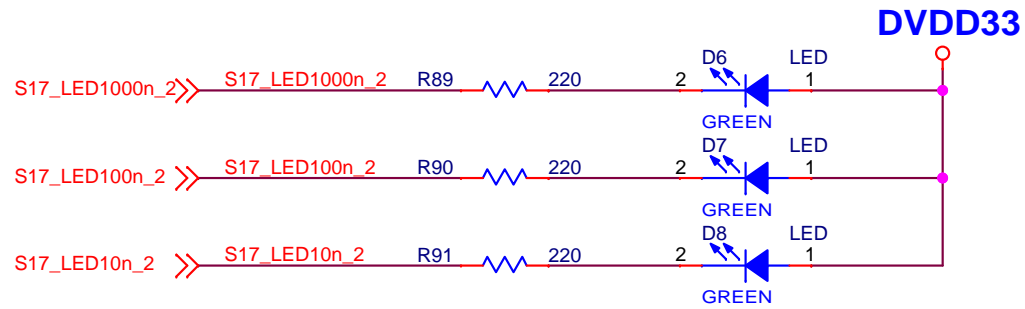
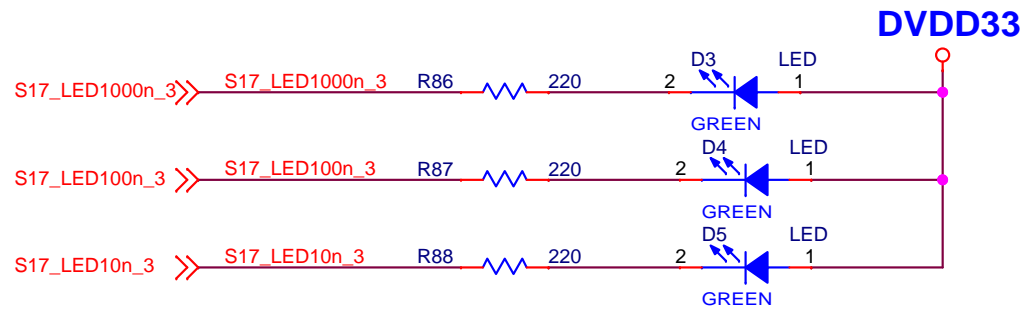
- (1) LX trace layout will impact the packet lost of PI(MAC1+PHY0).
- (2) LX trace doesn't change to any layer. So, please keep it at top-layer.
- (3) LX trace length is as short as possible and a large area. L2's DVDD 1.1V need also a large copper area.
- (4) Any trace, power and components don't close to LX trace in particular all 3.3V power and P1's twist-pair.
- (5) Any trace, power and components don't rout under LX trace / pin.


Note 3:

For VDD33_SVR(pin-A86) layout suggestion: (Please follow the below suggestion)

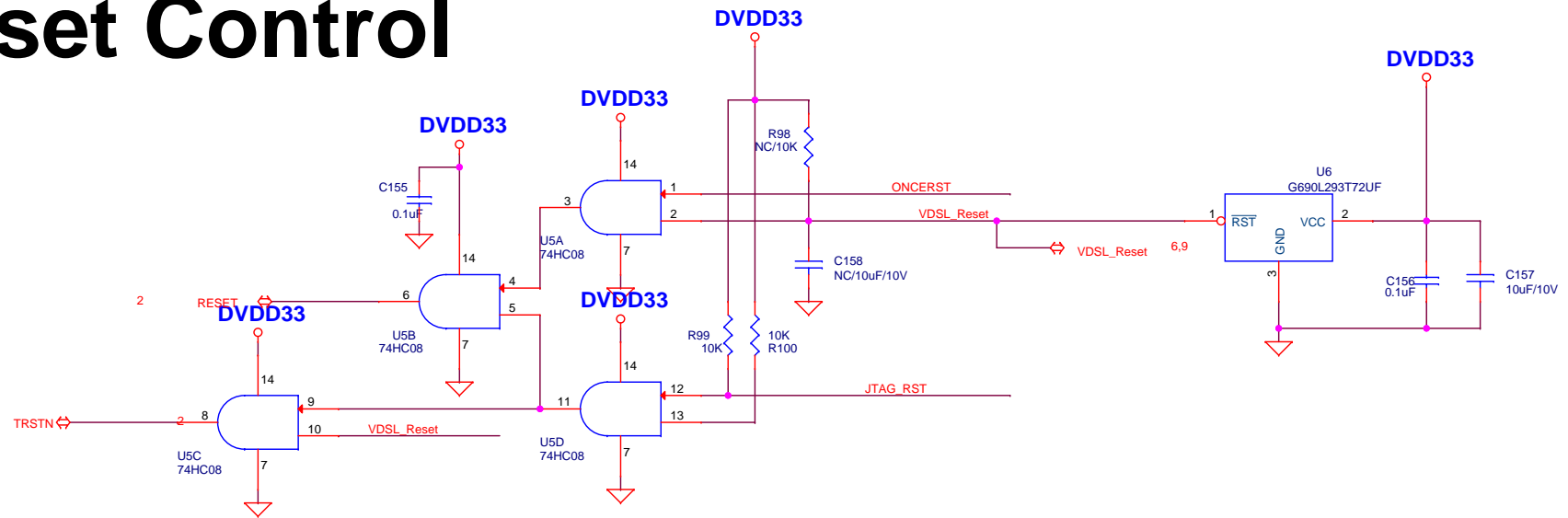
- (1) VDD33_SVR trace width >= 15mil.
- (2) The via of VDD33_SVR don't close to L2/LX trace.



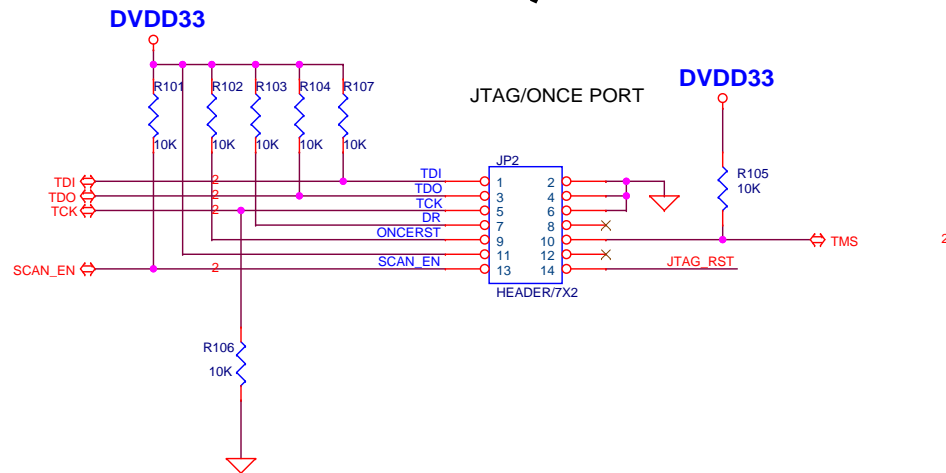


		
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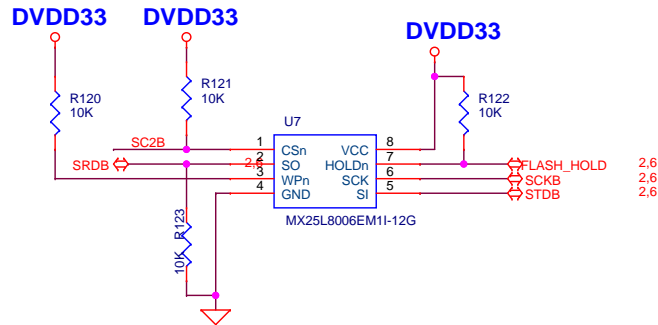
Reset Control



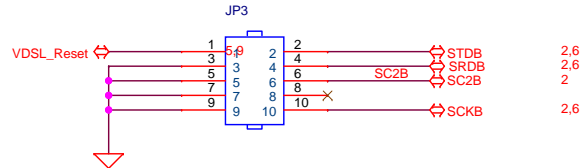
ONCE PORT/JTAG



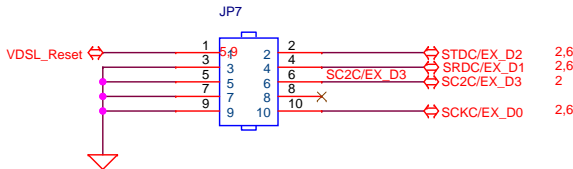
SPI Flash BOOTLOAD



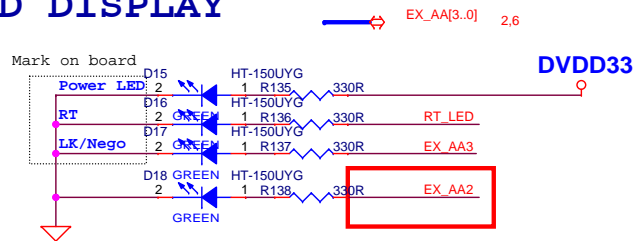
SPI Flash Programmer/EYEBOS CONNECTOR



SERIAL PORT C

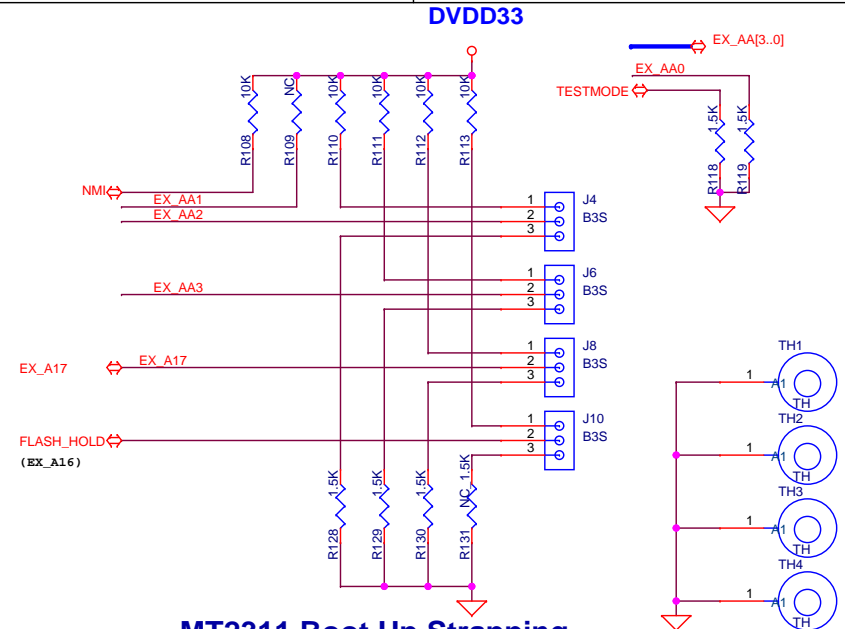
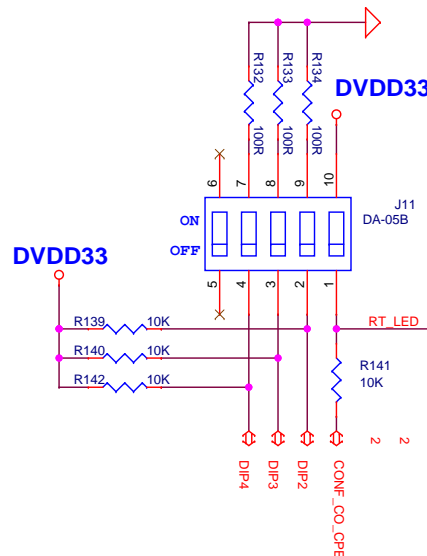
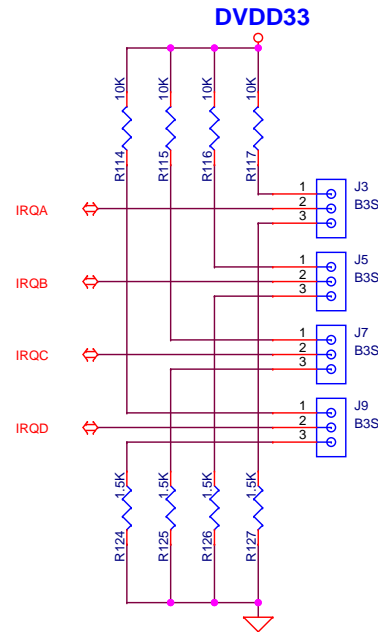


LED DISPLAY



LK/Nego LED:VDSL status led

Idle: slow blinking
Training: fast blinking
Showtime: continuous light
Packet transmit :fast blinking(option)



MT2311 Boot Up Strapping

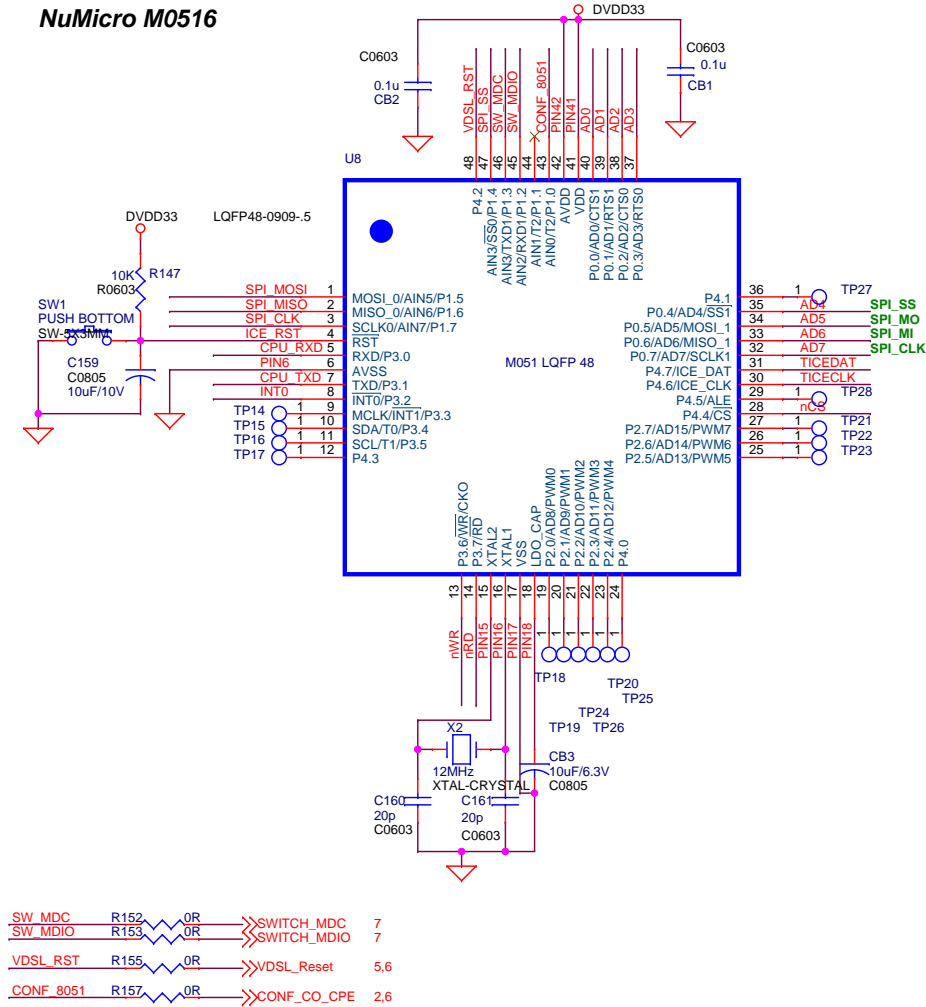
Pin Name	Description	Value=0	Value=1
EX_AA3	BIST	Disable	✓ Enable
IRQ[A,B,C,D]	BOOT FROM	✓0000 : SPI flash 1110 : 8bit HPI mode(CPU) 0101 : EBM Mode 0010 : SPI Slave Mode	
EX_[A17,A16]	EBM BOOT MII mode	00 : SMII 01 : MII 10 : GMII 11 : RGMII	
EX_A16	HPI Mode	8 bit mode	24 bit mode
EX_A17	HPI Mode	single strobe	dual strobe
EX_A17	SPI Slave Mode	HPI	SPI

- 1 TV1
- 1 TV2
- 1 TV3
- 1 TV4

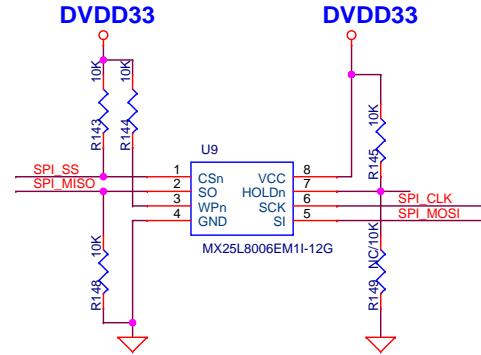
METANOVA

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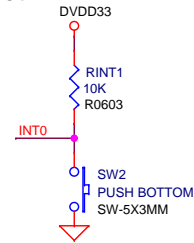
NuMicro M0516



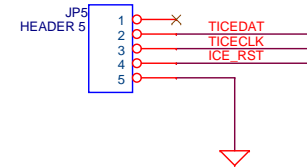
SPI Flash



Reset

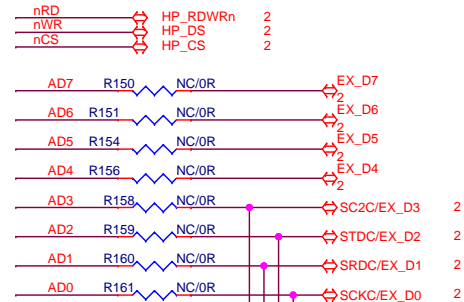


ICE INTERFACE

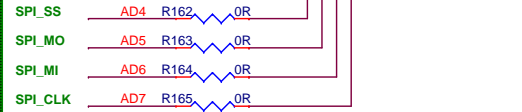


MT2311 boot and manager

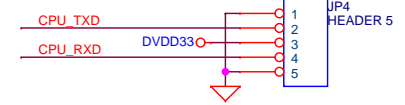
HPI mode



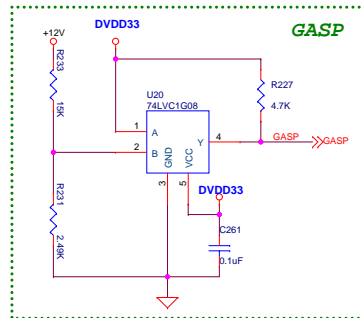
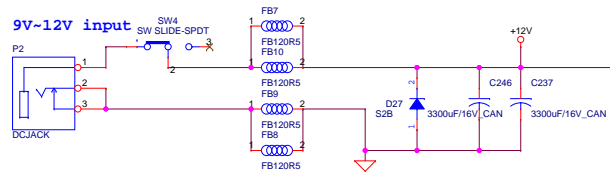
SPI mode



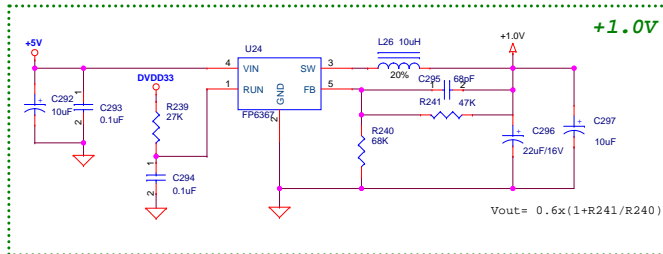
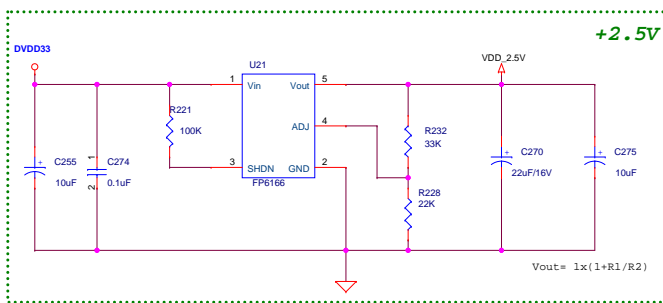
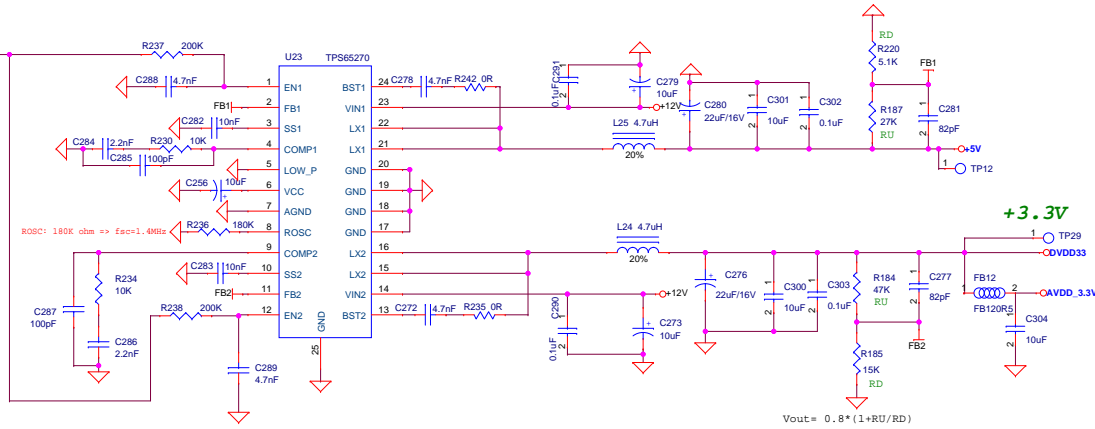
CPU CONSOLE



METANOIA



2.9



+5V

+3.3V

+2.5V

+1.0V

METANOIA

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Revision History

EVB2311-BA-N V1.0	<ul style="list-style-type: none">.Remove 1.1V Power Supply.Due to remove 1.1V Power Supply and AR8327 bug , Switch(RJ45) first port is invalid..Fix TDI issue. TDI pull-up by 10k ohm
EVB2311-BA-N V1.1	<ul style="list-style-type: none">.Use TPS65270(TI) Power IC
EVB2311-BA-N V1.2	<ul style="list-style-type: none">.Increase PortC interface.Add R34.Add R17

		
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